



Keynotes & Tutorials 2010

June 3rd: Keynote 1

Masaki MOMODOMI
Technology Executive, Flash Memory
Toshiba Corporation



Future technology and application of NAND flash memory

NAND flash market has been growing rapidly for these several years. There is even stronger demand for high capacity with affordable price for newer flash applications. But beyond 30nm technology of NAND flash memory has many difficulties. This talk will be about future device and circuit technologies including 3D-structure flash memory and its application and market analysis.

Masaki MOMODOMI has been Technology Executive of Flash Memory at Toshiba Semiconductor Company in Toshiba Corporation for 2 years. His responsibility is NAND flash and other non-volatile memory technology development.

He joined the Toshiba Research and Development Center of Toshiba Corporation in 1980. Since 1987, he has been working on the circuit design and device development of NAND flash memory.

Masaki MOMODOMI received the B.E degree in electronic engineering from Kyushu University, Fukuoka, Japan.



Keynotes & Tutorials 2010

June 4th: Keynote 2

Jean Luc JAFFARD
Emerging Markets and Image Signal Processing
Business Unit Director
Imaging Division
ST Microelectronics



Imaging market Evolution and its products & technological implications

Imaging market has been booming over the past years mainly fuelled by the wide adoption of Imaging technologies inside mobile phone. The purpose of this presentation is to show the implication of such a quick evolution to Imaging technologies both in term of methodology and products.

The Future Evolution and its implications in term of development techniques and products will also be addressed

Jean Luc Jaffard Graduated from Ecole Supérieure d'Electricite, France. In 1979 he joined Thomson Semiconductor (now STMicroelectronics) as mixed signal designer and has been involved in many consumer products developments such as analog TV core, remote controller, low noise VCR amplifiers, Audio and Video switches, teletext decoder. From 1990 to 1996 he was TV division design manager.

From 1996 to 1999 he initiated the Imaging activity at STMicroelectronics and contributed to the acquisition of VLSI Vision Limited. From 1999 to 2007 he had multiple activities within ST Imaging division mainly in product development

From 2007 to 2010 he has been Deputy General Manager of ST Imaging division and had the responsibility of the advanced technology developments for the division. He is now Business Unit Director in charge of Emerging Markets and Image Signal Processing inside ST Imaging Division



Keynotes & Tutorials 2010

June 2nd: Tutorial 1 - Dr. Sani Nassif - IBM



Characterization and Prediction of Technology Variability

As the semiconductor industry continues to scale silicon technology beyond the 22nm node, and in the absence of a clear alternative to silicon emerging, it becomes ever more important to understand the potential sources and magnitudes of manufacturing variability. This variability has always been important from the point of view of performance, but is projected to grow to the point where it is expected to impact correctness as well. For highly dense and regular structures like SRAM, this functionality impact is well documented and numerous device, circuit and system level responses (like supply boosting, error correcting codes, parity, and son on) have been developed to maintain SRAM yield and performance as further scaling occurs.

In this tutorial, we will review the essential sources of technology variability, show examples of how they can be characterized using special purpose test structures, as well as in-situ embedded structures. We will review some relatively recent data from 65nm and 45 nm processes which IBM has shared with researcher in several universities, and which helps show the breakdown of variability across lot, wafer, reticle, die and within die domains. We will show how the resulting characterization lends itself to representation in terms of spatial dependence, and finally close with some predictions for the future of variability down to the 12nm node.

Dr. Sani Nassif received his Bachelors degree from the American University of Beirut in 1980, and his Masters and PhD degrees from Carnegie-Mellon University in 1981 and 1985 respectively. He worked at Bell Laboratories until 1996 then joined the IBM Austin Research Laboratory where he currently manages the Silicon Analytics department, which is focused on design/technology coupling and includes activities in model to hardware matching, simulation and modelling, statistical modelling, statistical technology characterization and similar areas. He has authored numerous conference and journal publications, received several Best Paper awards (IEEE Trans. CAD, ICCAD, DAC, ISQED, SEMICON and ICCD), authored invited papers to ISSCC, IEDM, ISLPED, HOTCHIPS, and CICC, and given Keynote and Plenary presentations at Sasimi, ESSCIRC, BMAS, SISPAD, SEMICON and ATMOS. He is an IEEE Fellow (2008), a member of the IBM Academy of Technology, a member of the ACM, and has a total of 44 patents.



Keynotes & Tutorials 2010

June 2nd: Tutorial 2 - Dr. Keith Bowman - INTEL

Mitigating the Adverse Effects of Parameter Variations on Logic Design



Managing the impact of device and circuit parameter variations on performance and power is one of the primary challenges in microprocessor design. Parameter variations may be categorized based on the temporal scale (static and dynamic) and the spatial scale (die-to-die and within-die). Static variations are induced from fluctuations in the manufacturing process. Dynamic variations result from environmental and workload changes that occur during the microprocessor operation. Die-to-die (D2D) variations affect transistors and interconnects on a die equally. Conversely, within-die (WID) variations induce different electrical characteristics across a die. In this tutorial, the major sources of static and dynamic parameter variations, consisting of D2D and WID components, are described. Based on statistically-based models of microprocessor performance and power, the adverse effects of static variations on the performance and power distributions are elucidated. Validated with measured data, these models reveal that (i) WID variations directly impact the performance mean and the power median, and (ii) D2D variations impact the performance and power variances. Adaptive supply voltage (V_{cc}) and body-bias compensation circuits are presented as examples of variation-tolerant logic designs that reduce the effects of static D2D and WID variations on performance and power.

Dynamic variations further degrade the performance of conventional microprocessors by requiring a clock frequency (F_{clk}) guardband to ensure correct functionality within the presence of worst-case dynamic variations. Consequently, these inflexible designs cannot exploit the opportunities for higher performance by increasing F_{clk} or lower energy by reducing V_{cc} during favorable operating conditions. Since most systems usually operate at nominal conditions where worst-case scenarios rarely occur, these infrequent dynamic variations severely limit the performance and energy efficiency of conventional designs. In this tutorial, a resilient microprocessor design is presented to mitigate the F_{clk} guardband for dynamic variations to maximize throughput or energy efficiency. A resilient design is a system with error-detection and error-recovery capabilities to maintain overall correct system functionality within the presence of errors. Resilient circuits enable the microprocessor to operate at an F_{clk} determined by nominal operating conditions. When dynamic variations induce a timing error, the error is detected and corrected to maintain proper logic functionality, thus effectively eliminating the F_{clk} guardband for dynamic variations. Silicon measurements from a 45nm test-chip indicate that resilient circuits enable a 41% throughput gain at equal energy or a 22% energy reduction at equal throughput, as compared to a conventional design.

Dr. Keith A. Bowman received a B.S. degree from North Carolina State University in 1994, and M.S. and Ph.D. degrees from the Georgia Institute of Technology in 1995 and 2001, respectively, all in electrical engineering. From 2001 to 2004, he worked in the Technology Computer-Aided Design (TCAD) Group at Intel Corporation, where he developed and supported statistical-based models, methodologies, and software tools to predict microprocessor performance and power variability. Since 2004, he has worked in the Circuit Research Laboratories (CRL) at Intel, where his current research focuses on the development of circuit design solutions to mitigate the impact of parameter variations on circuit performance and power.



Keynotes & Tutorials 2010

**June 2nd: Tutorial 3 - Pr. Mitsumasa KOYANAGI
Tohoku University**



3-D Integration Technology and 3-D LSIs

In this tutorial talk, 1) 3-D integration technology, 2) 3-D hetero-integration and super-chip, 3) 3-D LSI design, and 4) Testing and dependability of 3-D LSIs are discussed. Firstly, key technologies for 3-D integration, TSV formation, microbump formation, chip or wafer stacking, are discussed. Then a super-chip integration technology for a hetero-integration is described. A number of KGDs (Known Good Dies) are simultaneously aligned and bonded onto a wafer or chips using a new self-assembly technique in the super-chip integration. Thirdly design constraints for 3-D LSIs are discussed demonstrating 3-D memory design, 3-D image sensor design, 3-D reconfigurable LSI design, and 3-D processor design. Finally test algorithm and test circuit and dependability for 3-D LSIs are discussed.

Dr. Mitsumasa Koyanagi received the B.S. degree in electrical engineering from Muroran Institute of Technology, Japan, and the M.S. and Ph.D. degrees in electronic engineering from Tohoku University, Sendai, Japan, in 1969, 1971, and 1974, respectively. In 1974, he joined the Central Research Laboratory, Hitachi, Ltd., where he worked on research and development of MOS memory device and process technology, and invented a stacked capacitor DRAM memory cell which has been widely used in the DRAM production. Stacked capacitor DRAM was the first commercialized 3-D LSI. He employed high-k materials in DRAM for the first time in 1978. In addition, he fabricated MOS transistors with shallow junction using laser-annealing technology for the first time in 1979. From 1980 to 1985, he worked with the Device Development Center, Hitachi, Ltd. In 1985, he joined the Xerox Palo Alto Research Center, California, where he worked on research and development of submicrometer CMOS devices, poly-silicon thin-film transistors, and the design of analog/digital LSIs. In 1988, he joined the Research Center for Integrated Systems, Hiroshima University, as a Professor, where he worked on scaled MOS devices, three-dimensional (3-D) integration technology, optical interconnection, and parallel computer system specific for scientific computation. In 1992, he fabricated the smallest MOS transistor with a gate length of 70 nm. He proposed 3-D integration technology based on wafer-to-wafer bonding for the first time in 1989. Since 1994, he has been a Professor with the Department of Machine Intelligence and Systems Engineering (currently the Department of Bioengineering and Robotics), Tohoku University, where his current research interests include nano-CMOS devices, memory devices, lowvoltage and low-power integrated circuits, new intelligent memory for parallel processor systems, 3-D integration technology, optical interconnection, parallel computer system specific for scientific computation, real-time image processing systems and artificial retina chips, retinal prosthesis and brain implant devices, and brainlike computer systems. He has been researching 3-D integration technology and optical interconnection for more than 15 years. Dr. Koyanagi was awarded the 2006 IEEE Jun-ichi Nishizawa Medal, the 1996 IEEE Clelio Brunetti Award, the 2001 Award of Ministry of Education, Culture, Sports, Science and Technology, the 1994 SSDM (Solid-State Devices and Materials) Award, the 2004 Optoelectronic Technology Achievement Award (Japan Society of Applied Physics), the 1990 Okouchi Prize, etc.



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June 2nd: Tutorial 4 - Dr. Bernard DIENY

Spintronic: Physics, Technologies and Applications to MRAM, Mix Memory & Logic, and RF spin-oscillators



Spinelectronics is a very rapidly growing area of R&D that merges magnetism and electronics. Since the discovery of GMR (Giant magnetoresistance) in 1988, several breakthroughs have further boosted this field (spin-valves 1990, tunnel magnetoresistance (TMR) 1995, spin transfer 1996). Spinelectronics has found applications in read heads of hard disk drives (1998) and more recently in non-volatile standalone memories (MRAM=Magnetic Random Access Memory). MRAMs integrate CMOS components with magnetic tunnel junctions (MTJ). MTJ consist of two magnetic layers separated by a thin oxide barrier (most often MgO, ~1nm thick). When a bias voltage is applied across this trilayer, the transparency of the barrier to electrons strongly depends on the relative orientation of magnetization in the two magnetic electrodes. This results in a change of resistance of the junction which can reach 600% at room temperature. Thanks to the non-volatility brought by the magnetic character of the electrodes, these elements are ideally suited for memory applications. Freescale launched the first MRAM product in 2006 (4Mbit chip). In this technology, the switching of the magnetization in the MRAM cell is achieved by local pulses of magnetic fields. More recently, alternative write schemes have been proposed which offer good scalability at least down to the 22nm technological node. They are based on spin-transfer writing. It was predicted in 1996 and experimentally observed for the first time in 2000 that the injection of a spin polarized current of sufficient density in a magnetic nanostructure can be used to switch the magnetization of this nanostructure. Therefore, it became possible to switch the magnetic configuration in an MTJ from parallel (low resistance state) to antiparallel (high resistance state) and vice-versa by sending bipolar pulses of current directly through the tunnel junction. The ultimate scalability of MRAM is actually expected to be achieved by a combination of spin transfer and thermally assisted switching (TA-ST-MRAM). Beside standalone MRAM, this hybrid CMOS/MTJ technology can also find important applications in logic by allowing to intimately mix memory and logic functions (non-volatile logic). In particular, this may help reducing the power consumption of electronic systems. Spin transfer also yields interesting perspective of application in the field of RF components. Indeed it was shown that steady magnetic excitations can be induced in magnetic tunnel junctions under DC current. This allows designing frequency tunable RF oscillators in frequency range interesting for wireless communication.

Dr Bernard DIENY graduated from Ecole Normale Supérieure de Cachan in 1981. He carried out his PhD thesis at Louis Neel laboratory in Grenoble. Dr Bernard DIENY has been conducting research in magnetism for 28 years. He has been a key actor in the pioneer work on spin-valves in 1990-1991. In 1992, he joined the “Nanostructure and Magnetism” laboratory at CEA/Grenoble where he acquired a specialty in nanomagnetism and spinelectronics. In 2001, he co-founded “SPINTEC” in Grenoble, a public research laboratory devoted to spinelectronics and particularly hybrid CMOS/magnetic components for memories and logic applications, RF devices based on spin-transfer and ultra high density magnetic recording. Dr B.Diény is co-inventor of 40 patents and signed more than 250 scientific publications. He received an outstanding achievement award from IBM in 1992 for the development of spin-valves. His team was finalist of the European Descartes Prize for Research for his work on thermally assisted MRAM in 2006. He was nominated CEA Research Director in 2007 and was recipient of an advanced grant from the European Research Council in 2009. He is co-founder of a start-up company “CROCUS Technology” developing Thermally Assisted and Spin Transfer MRAM.