ICICDT 2008

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The fourth annual International Conference on Integrated Circuit Design and Technology (ICICDT) was held in early June at the Minatec facility in Grenoble, France. This conference, dedicated to fostering direct interaction between designers and technologists, marked its return to Europe with nearly 75 papers presented over two days. Held two years ago in Padova, Italy, and on alternate years in Austin, Texas, the conference has attracted papers from North America, Europe, and all over Asia, from industry and academia both. The purpose of the conference is to bring together designers - from architects to circuit designers – and technologists - from materials scientists to device specialists - so as foster interaction and ideally generate that flash of insight that creates breakthrough solutions to pressing problems.

While it is impossible to do justice to all the material presented, a few dominant themes recurred in much of the work – the impact of transistor variability, future devices, and technology optimization will be discussed in this report.

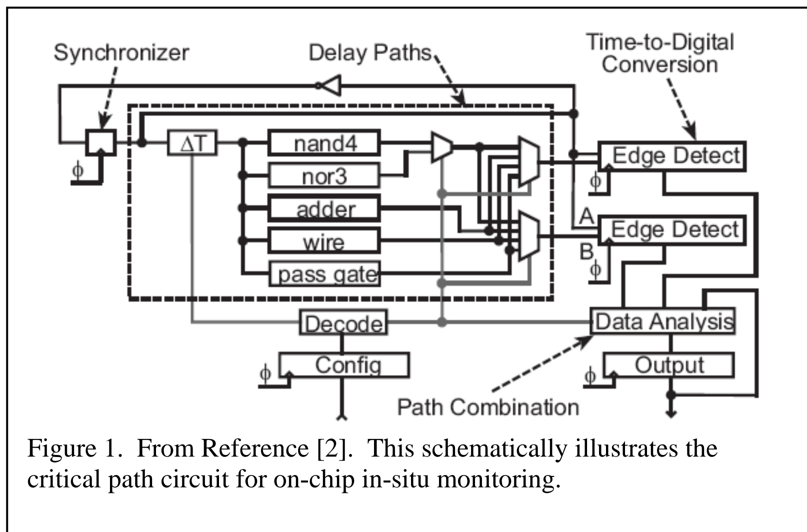

Figure 1. From Reference [2]. This schematically illustrates the critical path circuit for on-chip in-situ monitoring.

Variability has been recognized as one of the most troublesome aspects of newer technologies. While strain engineering and advanced dielectrics have enabled the transistor drive current to increase while decreasing the voltage and keeping the threshold voltage relatively constant, the reduced voltage overhead results in greater variation of delay with power supply variation, and threshold voltage tolerance. Furthermore, the reduced transistor size exacerbates the threshold variation associated with random dopant fluctuation, as well imposing stringent requirements on control of physical dimensions. Sophisticated design techniques can help alleviate the problems with transistor-level variability. In Ref. [1] the authors point out that the variability effect can be so large that, for example, a five-stage path can actually take more time than a six-stage path, and that care must be taken in identifying the true worst-case skew to be accommodated in the design. The authors from IBM in [2,3] describe techniques of on-chip measurements of path delay (Fig. 1) and clock skew,

to aid in tracking and compensating the large intra-chip, die-die, and voltage driven variations. Researchers from Intel describe methods of error recovery [4] to make chip functionality robust against these timing-related errors. Mathematic-based techniques to aid in understanding and planning for variability were discussed in [5-7] in papers from the University of Newcastle, Georgia Tech, and STMicroelectronics, respectively (Fig. 2).

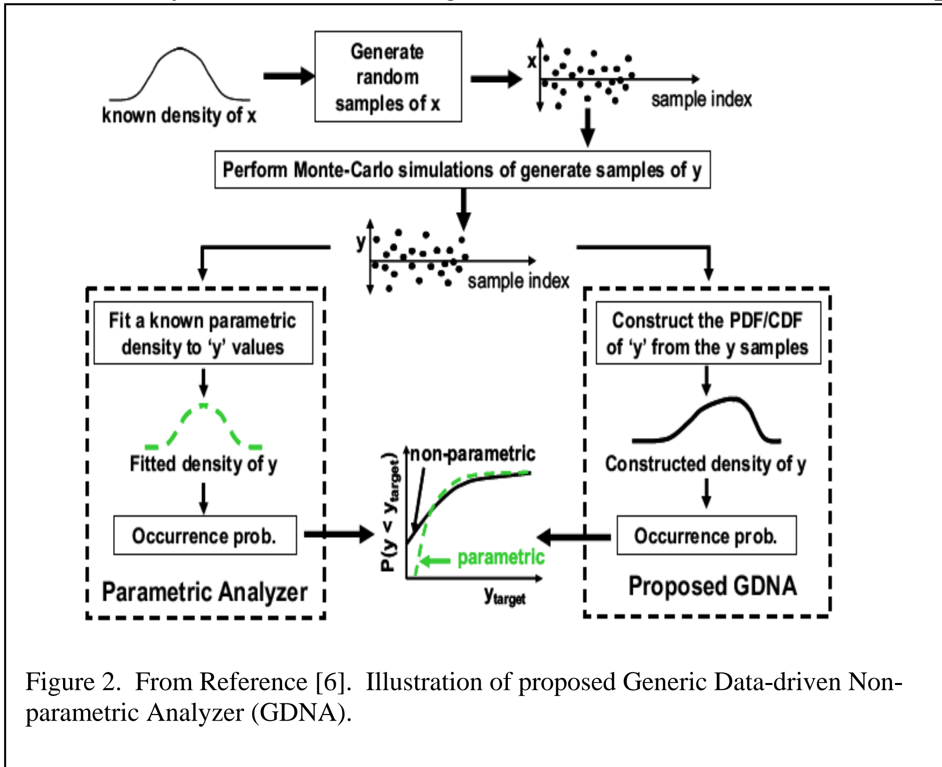

Figure 2. From Reference [6]. Illustration of proposed Generic Data-driven Non-parametric Analyzer (GDNA).

While taking different approaches, the authors of these papers recognize the Monte Carlo analysis of the sources of variation are computationally too cumbersome, and so offer a DOE-like approach to parametric sensitivity [5], a means of estimating a probability density function without assuming a functional form [6], and efficient estimation of the probability density function of the leakage [7].

While the design community has been working to make chips robust in the face of large variations, the technologists have not been idle. High-dielectric insulators and metallic gate material reduce the effect of random dopant fluctuation by reducing the effective oxide thickness in addition to improving drive current, enabling electrostatic scaling, and relieving the gate leakage roadblock. Further improvement in variability can be obtained by eliminating the dopant entirely. The threshold voltage of a Fully-Depleted SOI (FDSOI) transistor is determined by the gate

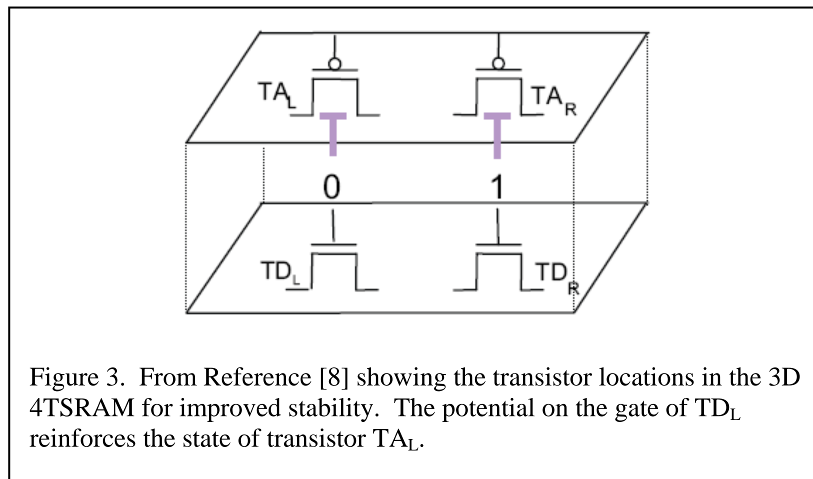

Figure 3. From Reference [8] showing the transistor locations in the 3D 4TSRAM for improved stability. The potential on the gate of TD_L reinforces the state of transistor TA_L.

work function and the body thickness, not doping atoms – there is therefore no random dopant fluctuation effect. A number of device structures are candidates for 22nm and beyond. Virtually all are some form of multiple-gate option. Aside from improved short-channel behavior, interesting things may be accomplished by manipulating the back gate. The authors from LETI in [8] describe how a 3-D structure can be suitably arranged such that the backbias effect acts so as to reinforce the state of the cell and enable a compact 4T SRAM cell (Fig. 3). An improved SRAM sense latch using the backgate effect is described in [9], and leakage reduction in a FINFET cell is discussed in [9] (Fig. 4) in a paper from NAIST in Japan. All prognostications of the future transistor seem to contain some form of SOI; the question seems to be not if, but only when, and in what form it will become dominant.

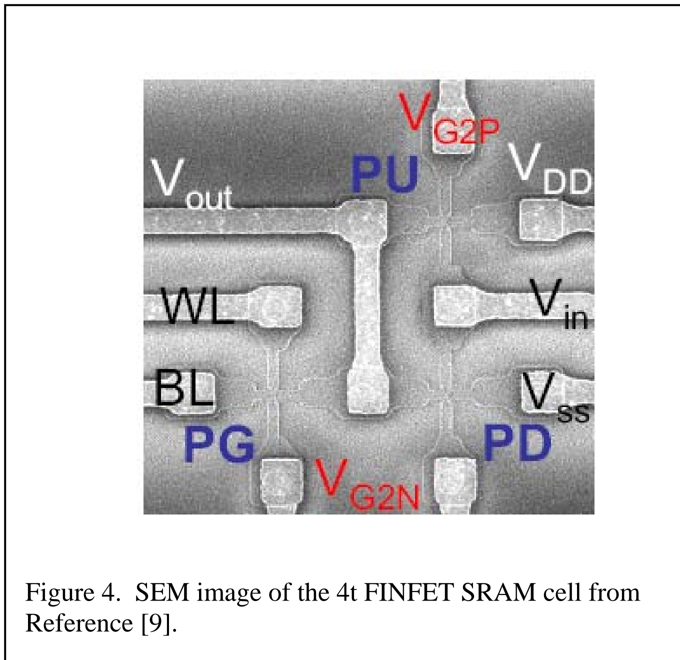

Figure 4. SEM image of the 4t FINFET SRAM cell from Reference [9].

Two presentations [10, 11], from Qualcomm and from NXP, were specifically directed to developing formalisms for technology assessment at the system level. The traditional path of detailed process definition leading to detailed spice models based on hardware, followed by library generation, followed by chip synthesis, is too slow and cumbersome to enable optimization of the technology for the specific application. By the time such a sequence of operations has occurred, the option to reshape the technology has all but passed, and the time for

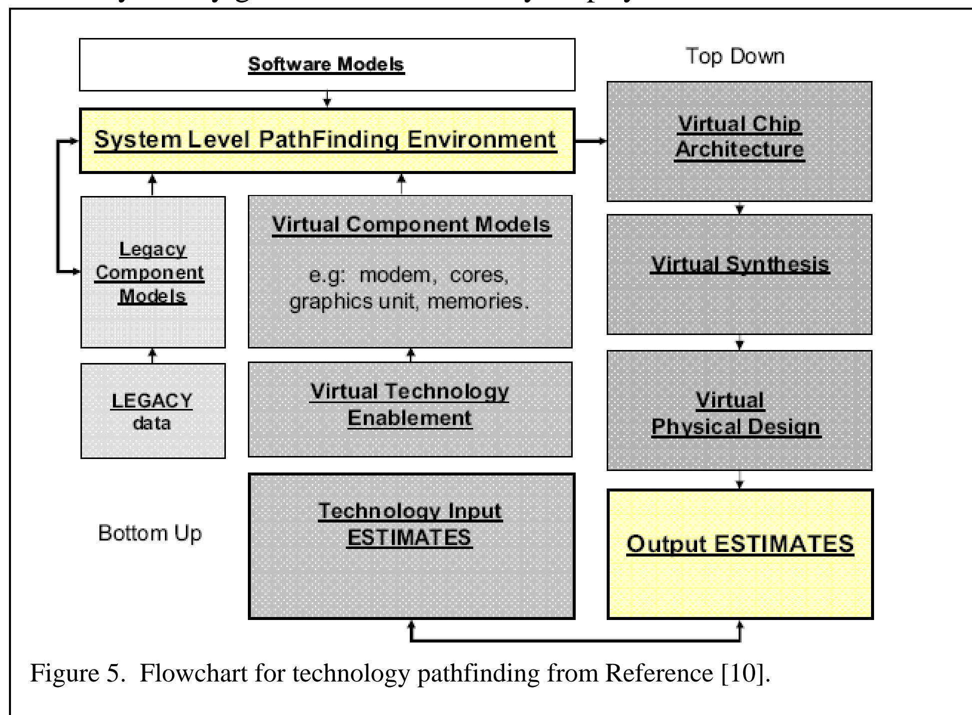

Figure 5. Flowchart for technology pathfinding from Reference [10].

the design to react to new challenges or opportunities has also been lost. While such "lookahead" activity has of course always taken place at the leading edge of technology, both sets of authors stress establishing a repeatable, documented flow to the process of technology assessment (Fig. 5).

The brief descriptions above can hardly summarize the few points expounded upon, and the context here can hardly allow for the full enumeration of all of the other topics covered in the conference. Topics such as RF devices, high-k dielectrics, new memory structures, and soft-error reliability were also addressed in some detail,

The ICICDT conference offers an unusual opportunity for technologists to interact with designers, and each to comprehend the others' perspective. A successful collaboration has been concluded for 2008, and planning is well underway for the 2009 conference in Austin.

References

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