



Call for Papers

Paper Deadline: March 1st, 2010

**International Conference on IC Design & Technology
Grenoble, France; June 2 – June 4, 2010**



As IC design & process technology continue to advance for increased performance, lower power, and accelerated time-to-market, the engineering activities, traditionally separated along the boundary of design and process technology, will have difficulties in meeting the shrinking window of product optimization tasks. The International Conference on IC Design & Technology provides a forum for engineers, researchers, scientists, professors and students to cross this boundary through interactions of design and process technology on product development & manufacturing. The unique workshop style of the conference provides an opportunity to technologists and product designers to exchange breakthrough ideas and collaborate effectively. Two days of technical presentations and workshops will be preceded by a one-day tutorial program of value to both the expert and the beginner.

The venue of 2010 ICICDT will be Minatec, Parvis Louis Néel, 38054 Grenoble, France. <http://www.ICICDT.org>

Papers are solicited on:

- Design approaches including system, circuit and EDA to manage power, leakage, process variation, signal integrity, reliability, yield, and manufacturability.
- Advanced VLSI design, including embedded and host processors, ASICs, memories sub-system, analog and mixed-signal circuits.
- Multicore System-on-Chip (SoC), System-in-Package (SiP), and IP reuse for fast design closure.
- Advanced materials, advanced metallization, and 3D interconnection as both, novel interconnect, scheme for future MPUs and approach for realization of SoCs.
- Process and circuit technology for advanced memories: ReRAM, PRAM, MRAM, FeRAM, PRAM, eDRAM, Nanocrystal Memory, Flash, etc with emphasis on reliability.
- Advanced transistor structures for bulk, multiple Gate, FDSOI, PDSOI, SSOI, SiGe, etc technologies
- RF & analog properties of advanced devices (MOS, Bip, MEMS ...), RF, mmW & analog circuits on advanced technologies (planar, heterogeneous, 3D...)
- New gate materials for adjusting V_t , enhanced mobility & scalability, low leakage, and low power.
- SER, thermal, leakage, Plasma-Induced Damage (PID), reliability, yield, etc effects on advanced transistor structures and circuits.
- Simulation & modeling on advanced process, device & circuit.
- Nanotechnology materials, devices and circuits.
- ESD protection circuitry, mixed-voltage-tolerant I/O design, high speed and low power I/O buffer
- Emerging IC technologies and circuits crossover such as organic IC's, integrated sensors and actuators.
- High Power, High Voltage devices and technology

Prospective authors are invited to submit a camera-ready paper of maximum four pages in length, including figures and references. The authors should obtain paper submission guidelines from <http://www.ICICDT.org>. Accepted/Invited papers will be included in the proceedings of the conference (available on CD-ROM). **Presented paper will be published in IEEE Xplore and accepted paper must accompany by a non-refundable registration fees.** Paper submission deadline is **March 1, 2010**.



Conference Format

ICICDT features a popular and unique format structured to maximize face-to-face interaction. An abbreviated synopsis of each paper is presented in a plenary session, following which a workshop-style forum allows for deeper give-and-take communication on an individual basis. Many participants in previous years have commented that this interaction is very rewarding.

Contact Information

For further general information or assistance in selecting a subject area, please contact:

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