International Conference on IC Design and Technology (ICICDT)

May 23rd – 25th, 2017
Austin, Texas, USA
www.icicdt.org

Tutorial Program

Tuesday, May 23rd, 2017

9:30AM – 10:30AM: Tutorial 1

"Optical Interconnection with Si Photonics Platform for IoT Era"

Chief Manager Tohru Mogami (PETRA)

Optical interconnect is a promising technology for wide-band and large-capacity data communications for IoT era, instead of electrical interconnect, which can be one of the issues in the advanced IoT technology. For optical interconnect, Si photonics devices and technology based on Si CMOS technology is a key to produce integrated photonic chips. Si photonics technology has the advantages of easy device integration and high-speed and large-capacity performance on a chip. This tutorial addresses the recent development of Si photonics for short-distance optical interconnect in IoT era. We will find state-of-the-art Si photonics device characteristics and integration technology. Future Si photonics technology will be discussed.

Tohru Mogami is Chief Manager of IPECST Project, which is performing in research and development for new generation photonics device and networking technology by utilizing Si photonics technology, at PETRA, in Tsukuba, Japan. He oversees the process and device design, process flow and integration of Si photonics chips. He received the B.S. in physics, and the M.S., and Ph.D. in electrical engineering, all from Tohoku University, Japan. He joined NEC Corporation in 1982. He has been engaged in research and development of VLSI processing and device technologies. He has managed and contributed to the research and development of multiple-generation CMOS technologies. From 2006 to 2011, he was at Selete Inc., Japan, where he was the general manager of MIRAI Project. In this project, he contributed to the variation control technologies of transistors, and the development of CNT interconnects and optical interconnects. He is an IEEE Fellow, a Fellow of the Applied Physics Society, and a Fellow of the IEICE.

10:30AM – 11:00AM: Coffee Break

11:00AM – 12:00PM: Tutorial 2

"Near-/Sub-threshold Circuit Design: Opportunities and Challenges"

Prof. Masanori Hashimoto, Osaka University, Japan

Voltage scaling is the most effective approach to reduce power dissipation, and aggressive scaling to near- or sub-threshold voltage is drawing attention for not only IoT but also high performance applications. This tutorial addresses the opportunities of near-/sub-threshold circuits and introduces state-of-the-art developments. Next, we focus on design challenges. Near-/sub-threshold circuits are extremely sensitive to manufacturing and environmental variability and they are susceptible to soft errors. This tutorial also discusses robust subthreshold circuit design from variability and soft error perspective.

Masanori Hashimoto received the B.E., M.E., and Ph.D. degrees in communications and computer engineering from Kyoto University, Kyoto, Japan, in 1997, 1999, and 2001, respectively. Now, he is a Professor with the Department of Information Systems Engineering, Osaka University, Osaka, Japan. His current research interests include computer-aided design for digital integrated circuits, design for manufacturability and reliability, timing and power integrity analysis, reconfigurable computing, soft error characterization and low-power circuit design.
Dr. Hashimoto received the Best Paper Awards of ASP-DAC and IEICE Transactions in 2004 and 2016, respectively. He was on the technical program committees of international conferences including DAC, ICCAD, ITC, Symposium on VLSI Circuits, ASP-DAC and DATE. He serves/served as an associate editor for IEEE Transactions on VLSI Systems and Circuits and Systems I.

12:00PM – 1:30PM: Lunch

1:30PM – 2:30PM: Tutorial 3

"Advanced devices and materials for 7 nm node and beyond"

Prof. Shinichi Takagi (The University of Tokyo)

Traditional CMOS scaling has confronted a variety of difficulties, attributed to essential Si material properties as well as practical problems such as limitation of lithography, performance variation, cost and so on. Here, reduction in both device foot print and power consumption is the most serious concerns for realizing future integrated systems. Ultrathin body channels and multi-gate structures, resulting in FinFETs and nanowire MOSFETs, are indispensable in order to minimize short channel effects and to decrease the device size.

On the other hand, the reduction in power consumption requires the decrease in supply voltage, which can be realized by two strategies. One is the increase in on-current due to higher mobility (velocity) channel materials with low effective mass. The other is the development of steep slope devices with lower sub-threshold swing than CMOS. From these points of view, tremendous efforts have been devoted to on improvements and optimization of MOS-based logic device structures and materials used there in these one or two decades.

This tutorial will deliver the current status and future prospects of these advanced MOS device technologies for 7-nm technology node and beyond with an emphasis on device structures and materials for low power applications. The content can include typical examples of advanced CMOS, Ge/III-V CMOS, steep slope devices such as tunneling FET and negative capacitance gate MOSFET, vertical integration of CMOS and devices based on 2D-based materials.

Shinichi Takagi was born in Tokyo, Japan, on August 25, 1959. He received the B.S., M.S. and Ph.D. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, in 1982, 1984 and 1987, respectively. His Ph.D. thesis involved the study on the surface carrier transport in MISFETs based on III-V semiconductors.

He joined the Toshiba Research and Development Center, Kawasaki, Japan, in 1987, where he has been engaged in the research on the device physics of Si MOSFETs, including the carrier transport in the inversion layer, the impact ionization phenomena, the hot carrier degradation and the electric properties of Si/SiO_2 interface. From 1993 to 1995, he was a Visiting Scholar at Stanford University, Stanford, CA, where he studied the Si/SiGe hetero-structure devices. Since returning to the ULSI Research Laboratories, he was also engaged in the physics and technology of the reliability of SiO_2, ferroelectric devices and strained-Si MOS devices. He worked for the MIRAI Project as the leader of Ultra-High Performance New Transistor Structures Theme from 2001 to 2007. In October 2003, he moved to the University of Tokyo, where he is currently working as a professor in the department of Electrical Engineering and Information Systems, School of Engineering. He has authored and co-authored more than 840 papers in technical journals and international conferences on these and have received 16 awards including IEEE Andrew S. Grove Award (2013) and IEEE Paul Rappaport Award (2014). His recent interests include the science and the technologies of advanced CMOS devices using new channel materials such as strained-Si, Ge and III-Vs.

Dr. Takagi served on the technical program committee on several international conferences including International Electron Device Meeting, Symposium on VLSI Technology, International Reliability Physics Symposium, International Conference on Solid State Device and Materials and International Solid State Circuits Conference. He is a member of the IEEE Electron Device Society and the Japan Society of Applied Physics.

2:30PM – 3:00PM: Coffee Break

3:00PM – 4:00PM: Tutorial 4

"Ensemble Monte Carlo methods for nanoscale Si and III-V n-channel FinFETs; non-equilibrium degenerate statistics, quantum-confined scattering & more"

Prof. Leonard F. Register, The University of Texas at Austin, , USA

Particle-based ensemble semi-classical Monte Carlo (SCMC) remains a benchmark in semiconductor device research, because of combination of relative computational efficiency, first-principles transport physics, and the ready ability to model scattering. The latter contributes not just to injection efficiencies, but screening of potential wells, thermalization of carrier distributions (particularly among energy valleys), and source drain-resistance. However, particle-based ensemble semi-classical Monte Carlo (MC) methods must employ quantum corrections (QCs) to address quantum confinement and degenerate carrier populations to model today's and tomorrow's ultra-scaled MOSFETs. We describe the most complete treatment of quantum confinement effects and carrier degeneracy in a three-dimensional (3D) MC device simulator to date, and illustrate their significance through simulation of n-channel Si and III-V FinFETs. Far-from-equilibrium degenerate statistics, QC-based modeling of surface-roughness scattering, quantum-confined phonon and impurity scattering are considered, in addition to quantum confinement-induced redistribution of charge carriers in real-space and momentum-space. The used of use of fractional "subcarriers" also minimizes classical carrier-carrier scattering that is incompatible with degenerate statistics, as well as providing improved statistics. FinFET simulations are used to illustrate the contributions of each of these QCs. As an illustration, we show how collectively these modeled quantum effects can substantially reduce and even eliminate otherwise expected benefits of a considered In0.53Ga0.47As FinFET over Si but otherwise identical Si FinFET, despite lower bulk electron masses and higher mobilities and thermal velocities in In0.53Ga0.47As.

Leonard Franklin Register is the J. H. Herring Centennial Professor in Engineering within the Electrical and Computer Engineering Department at the University of Texas at Austin, a member of the Microelectronics Research Center. He is a Fellow of the Institute of Electrical and Electronics Engineers (IEEE) and a Fellow of the American Physical Society (APS). Register is a device theorist whose research is focused on understanding and modeling nano-scale electronic and magetoelectronic devices, and the essential physics underlying their operation. His current research interests include alternative materials, state variables and switching methods for beyond CMOS devices and memory; alternative materials and device geometries for CMOS; and quantum transport and quantum-corrected semiclassical transport toward the former.